Automated Test Outlook 2010

A Comprehensive View of Key Technologies and Methodologies Impacting the Test and Measurement

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La rápida tasa de crecimiento económico y tecnológico está forzando a muchas compañías a reevaluar las estrategias de test para encontrar un enfoque más optimizado. Como líder en test automatizad, National Instruments desea ayudarle a darle forma a su estrategia de test proporcionando información acerca de las tendencias más relevantes que tendrán más impacto de negocios en el 2010 y más adelante.

En el área de ESTRATEGIA DE NEGOCIO, NI predice un enfoque en:
ESTANDARIZACIÓN.- *El crecimiento acelerado a finales de los 1990s y mediados de los 2000 llevó a una falta de enfoque en uniformidad del sistema de prueba y reutilización. Hoy, el resultado es una mezcla de arquitecturas de sistemas de pruebas automatizadas y activos agravados por adquisiciones y fusiones.*
Organizando una estrategia de test alrededor de una plataforma de prueba común es una técnica probada para reducir costo de capital, incrementar reutilización, y reducir gastos operativos y de huella en sistemas de tests redundantes.

En el área de ARQUITECTURAS, NI predice un enfoque en:
TEST DE RF MULTICANAL.- *La migración a estándares de comunicación basados en tecnología de múltiples-entradas, múltiples-salidas (MIMO), tales como WLAN 802.11n, Mobile WiMAX, y 3GPP Long Term Evolution (LTE), está dirigiendo la próxima ola en la evolución de RF.*
Las compañías deben considerar arquitecturas de test RF multicanal optimizadas para evitar incremento en los tiempos de test y costes. Estas aplicaciones requieren un nuevo nivel de sincronización de fase coherente que va más allá de relojes de referencia y disparos de inicio de 10 MHz.

En el área de COMPUTACIÓN, NI predice un enfoque en:
COMPUTACIÓN PUNTO A PUNTO.- *La instrumentación definida por software da a los ingenieros acceso a petabytes de datos de medición en bruto. La computación punto a punto utiliza una arquitectura descentralizada para distribuir el procesamiento de datos y recursos a través de múltiples nodos de procesamiento.*
Los dos usos más probables en computación punto a punto son adquirir datos directamente de un instrumento y transferirlos hacia un módulo de arreglos de compuertas programables en campo (FPGA) para procesamiento en línea, o descargando los datos a otros sistemas de test u ordenadores de alto rendimiento.

En el área de SOFTWARE NI predice un enfoque en:
DISEÑO EMBEBIDO Y TEST.- *Los sistemas embebidos están proporcionando nuevos niveles de conveniencia y seguridad a consumidores y nuevas oportunidades profesionales a los ingenieros. A medida que estos sistemas se vuelven más sofisticados, las cadenas de herramientas y procesos para el diseño y prueba crecen volviéndose infinitamente más complejas.*
Hoy en día, los ingenieros deben refinar sus estrategias para superar las transiciones entre herramientas de diseño y prueba, las cuales resultan en la reescritura total del código de prueba, casos, y simulación, e interconexión de E/S de los modelos y E/S del mundo real.

En el área de E/S, NI predice un enfoque en:
INSTRUMENTOS RECONFIGURABLES.- *Mientras que las FPGAs han sido utilizadas por más de una década, los ingenieros rara vez tenían acceso a ellos. Las FPGAs deberían ser reprogramables para llevar los algoritmos definidos por el usuario directamente al hardware. Sin embargo, la mayoría de los ingenieros de test no tienen un conocimiento profundo de Verilog o VHDL.*
Afortunadamente, el crecimiento de las herramientas de diseño de alto nivel está cambiando las reglas de la programación FPGA con nuevas tecnologías que convierten diagramas de bloques gráficos – o incluso código ANSI C – en circuitería de hardware digital.

Debido al extraordinario interés de este artículo, reproducimos integramente su original en inglés.

"Our industry is evolving so quickly that it's difficult to stay current on the latest developments. The Automated Test Outlook will help educate you on the technologies, methods, and best practices that will drive innovation in test system design over the next five years" .
Eric Starkloff, Vice President, Product Marketing for Test, National Instruments

A Global Catalyst for the Automated Test Industry

Since 1976, companies around the world have relied on National Instruments products and services to build sophisticated automated test and measurement systems. By standardizing on NI tools, these test engineering organizations are improving the quality of their products while reducing costs.

These benefits have been realized by industry-leading companies including BMW, Lockheed Martin, Sony, and Texas Instruments.

While continuing to serve as today's leading authority in instrument control technologies, NI is driving innovation in test system design with software-defined instrumentation. This approach combines the advantages of open, industry- standard PC technologies, modular instrumentation, and proven instrument control options – all powered by the industry's most comprehensive and widely chosen test system software. Through this approach, test engineers achieve savings in capital equipment and system development with lower maintenance costs and faster execution.

An important part of National Instruments leadership is its involvement with multivendor consortia, including the PCI-SIG, PICMG, PXI Systems Alliance, and the IVI Foundation. These organizations impact business by delivering a common software and hardware architecture that simplifies commercial and test system development and provides vendor interoperability. National Instruments, join with partners industry-leading instrumentation vendors, such as Tektronix, to drive further advancements in the test and measurement industry. One of the latest innovations the collaboration between NI and Tektronix is a high-bandwidth of PXI Express digitizer that delivers unprecedented capability to the PXI platform. The product combines Tektronix's unique ASIC technology and high-bandwidth design experience with NI modular instrumentation, data streaming, and software expertise.

In addition to partnering with key instrumentation vendors, NI delivers this continuous improvement with a strong investment in R&D. NI reinvests more than 16 percent of revenue in R&D, which is significantly more than the industry average. These investments are balanced between providing higher performance and greater ease of use. The latest enhancements include targeting field-programmable gate arrays (FPGAs) and multicore processors as well as advanced precision and RF measurement capabilities. With these new products and technologies, test engineers can develop cost-effective test systems that are flexible enough to meet current and future application requirements.

A Technology and Business Partner

Test is a critical component of your product development and production process. It can improve a product's performance, increase quality and reliability, and lower return rates. It is estimated that the cost of a failure decreases by 10 times when the error is caught in production instead of in the field and decreases 10 times again if it is caught in design instead of production. By catching these defects and collecting the data to improve a design or process, test delivers value to your organization. Driving innovation into this process through technology insertion and best-practice methodologies can generate large efficiency gains and cost reductions.

We've found that one of the biggest challenges for test engineers and managers is staying current on the latest test trends. Keeping up with the changing technologies of the devices you design and manufacture is daunting enough; keeping up with all the technologies that drive test process improvements as well as new testing techniques is even harder.

National Instruments has a broad knowledge of technology trends and interacts with companies across many sectors, which gives us a unique vantage point on the test and measurement market. This view has enabled us to be a strategic partner with leading companies in identifying trends and industry best practices. We try to be as transparent as possible in providing this information to our users to help them make the best business decisions for their organizations.

The goal of the Automated Test Outlook is to both broaden and deepen the scope of these existing efforts. We are documenting the information from our own internal research and key customer engagements and making it publicly available for a broader audience of test engineers and managers who are influencing test strategy. Our desire is to help educate you and your teams and give you the information you need to make key technical and business decisions.

How We Arrived at the Trends

Predicting the future is hard work. Fortunately, we cast a wide net in terms of the inputs we use to arrive at the trends. As a supplier of test technology to more than 30,000 companies worldwide each year, we receive a broad range of feedback across industries and geographies. This broad base creates a wealth of quantitative and qualitative data to draw on.

We stay up-to-date on technology trends through our internal research and development activities. As a technology-driven company, we invest more than 16 percent of our revenue annually into R&D. But as a company that focuses on moving commercial technology into the test and measurement industry, our R&D investment is leveraged many times over in the commercial technologies we adopt. Thus, we maintain close, strategic relationships with our suppliers. We conduct biannual technology exchanges with key suppliers that build PC technologies, data converters, and software components to get their outlooks on upcoming technologies and the ways these suppliers are investing their research dollars. Then we integrate this with our own outlook. We also have an aggressive academic program that includes sponsored research

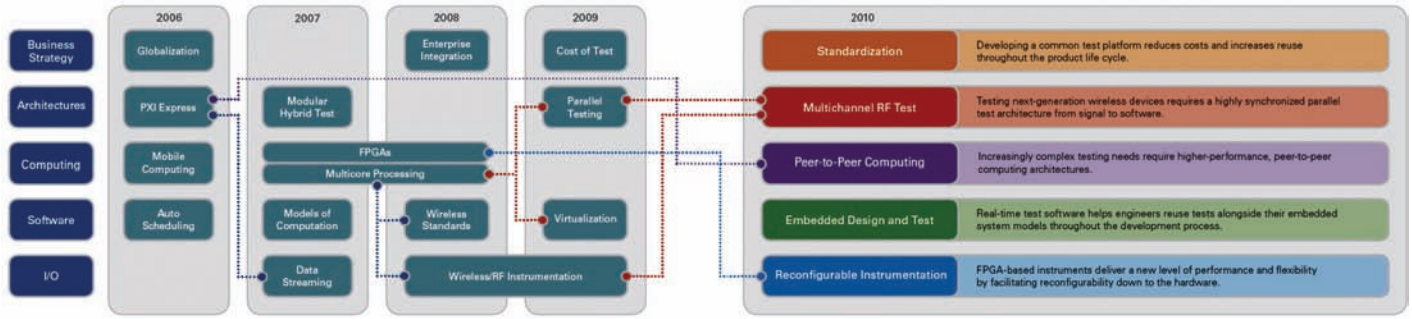

Figure 1. Automated Test Outlook Topics over the Past Five Years

across all engineering disciplines at universities around the world. These projects offer further insight into technology directions often far ahead of commercialization.

And, finally, we facilitate advisory councils each year where we bring together leaders from test engineering departments to discuss trends and to share best practices. These councils include representatives from every major industry and application area – from testing fighter jets to the latest smartphone to implantable medical devices. The first of these forums, the Automated Test Customer Advisory Board, has a global focus and is in its 10th year. We also conduct regional meetings, called Regional Advisory Councils, around the world. Annually, these events touch well over 300 of the top thought leaders developing automated test systems.

We've structured this outlook into five categories (see figure 1). In each of these categories, we highlight a major trend that we believe will significantly influence automated test in the coming one to three years. We update the trends in these categories each year to reflect changes in technology or other market dynamics. We will even switch categories if the changes happening are significant enough to warrant it.

As with our face-to-face conversations on these trends, we hope that the Automated Test Outlook will be a two-way discussion. We'd like to hear your thoughts on industry's technology changes so we can continue to integrate your feedback into this outlook as it evolves each year.

Standardization

Fast-paced growth in the late 1990s and mid-2000s intensified time-to-market pressures, which led to a lack of focus on test commonality and reuse.

The result many organizations face today is a mix of automated test system architectures and assets that is further compounded by the blending of companies and test systems through acquisitions and mergers. Companies are looking to reduce cost of test by optimizing people, processes, and technologies involved in their test system development, deployment, and operation. Organizing your test strategy around a common test platform is a proven technique for reducing capital cost, increasing reuse, and lowering the operational overhead and footprint of redundant test systems.

A lack of focus on test system commonality leads to non-standard test systems per product, per design phase, and per geographic location. The surplus of dedicated test equipment, development resources, and trained operator and support staff per station adds significantly to a company's cost of test. It also complicates asset management, slows ability to react to business needs, and minimizes leverage with strategic test vendors. Many companies are beginning to draw a hard line on this issue by requiring step function savings in their cost of test as opposed to incremental improvements.

Standardization strategies vary widely depending on the underlying business needs and existing test circumstances. Some focus on standardizing across product lines while others look at tester commonality across geographic regions. Emphasis on standardization and test reuse throughout the product lifecycle from design, validation and verification, to production is also becoming an important area to gain alignment. Companies are encouraged to consider at least two of the aforementioned areas of standardization to ensure significant results and sticking power of the standardization effort. In all cases, companies should look at their people, process, and technology assets and future investments to determine their optimal standardization strategy.

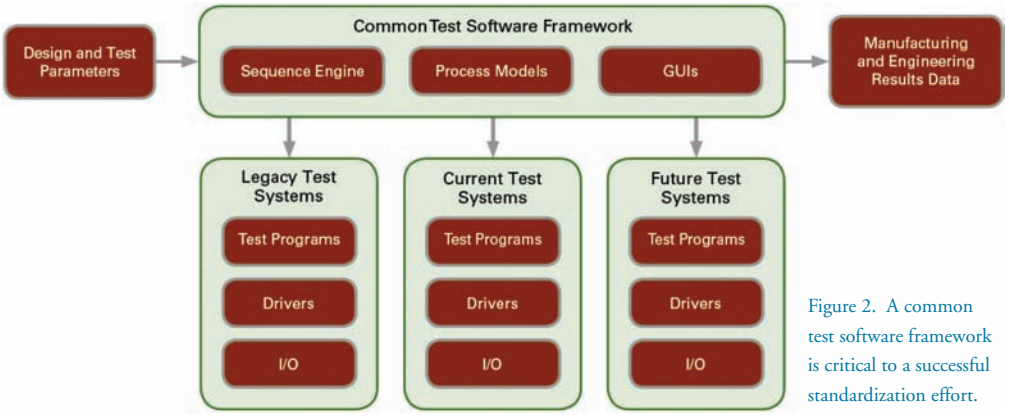

Figure 2. A common test software framework is critical to a successful standardization effort.

Defining the right level of standardization requires finding the proper balance between a rigid specification and no standard at all. Without a standard, it becomes difficult to adjust to production needs and can slow time to market due to the plethora of one-off systems and support requirements. It also makes it difficult to maintain quality control and gain leverage with suppliers. A rigid standard that fits every use case, on the other hand, is often over-designed and expensive. It is also difficult to secure adoption of a rigid standard because it is difficult for engineers to address exception use cases. The optimal solution often lies between the two extremes and requires defining a common core standard with permitted application extensions. Depending on the organizational needs, the common core could be an approved list of vendors or products, a chosen hardware platform, or a more complete platform tester. A standard hardware platform based on selected test capabilities and capable extensions provides the most flexibility for most companies. It is also allows for easier integration with existing and legacy testers because it provides a defined platform without being as rigid as a complete tester.

Moving forward, software is becoming an increasingly important part of test systems and a common software framework is the most critical for achieving a successful standardization effort (see figure 2). A common test software framework provides a universal interface between all test systems. The modular software architecture of

Global production test standardization allows Hella to maintain its high product quality in a cost-effective and scalable manner, helping us realize a 46 percent reduction in operational test cost and savings of an additional investment of a million euros every year.

Michael Follmann, Executive Vice President, Electronics Operations, Hella KGaA Hueck & Co.

MIMO technology is at the core of next-generation wireless networks, including fourth-generation cellular systems and wireless local area networks. Prototyping and testing these MIMO wireless communication systems will require a low-cost and adaptable multichannel RF architecture that supports comparable bandwidths, and a variety of modulation formats, and permits multichannel synchronization.

Professor Robert W. Heath, Jr., Ph.D., P.E., Department of Electrical and Computer Engineering, The University of Texas at Austin

the common test framework provides commonality across all of the test management related functions of test systems by sharing common process models, database and report logging, hardware abstraction layers, and operator interfaces. This modularity also ensures the ability to plug-in existing test scripts and programming to avoid re-hosting current and legacy testers. Moving forward with the development of standardized common core testers, it allows engineers to focus more on developing test sequences and I/O programming instead of having to develop the entire test management and enterprise connectivity solution as well.

Taking the proper steps to specifying a standard hardware platform is also very important. Defining a common set of hardware to satisfy a variety of test needs across products, regions, and design cycle phases can be a daunting proposition. One approach to greatly simplify this exercise is to focus on gathering the measurement needs instead of listing the capabilities of existing test systems. This helps to identify an optimized set of system requirements and lower overall cost whereas the latter approach tends to capture a superset of legacy requirements which are often no longer used or required.

Once a common hardware platform is defined additional measures can be used to help promote adoption and discourage off-platform deviations. A simplified procurement process for common core hardware kits and permitted application extensions is one example. Providing a dedicated support team to field questions about developing and supporting the common core platform is another. Documentation and example code also goes a long way towards easing adoption. Similarly, requiring similar levels of documentation and length exception review processes can help discourage deviating from the common core standard platform. In general, a good way to think about ensuring the adoption and longevity of a common core platform is to "treat it as a product" and its internal users as its customers. This helps frame the mindset for timely updates, resolving support issues, and providing closed-loop feedback on new feature requests.

Executing a well-planned standardization effort is proving to have significant business impact across all types of businesses and industries regardless of volume, mix, and number of sites. The primary business benefits include faster development time, increased reuse, smaller equipment footprint, and improved flexibility. Standardizing on a common core platform with a common software framework is a proven strategy for achieving a step function in optimization in companies resulting in a significantly lower overall cost of test.

Multichannel RF Test

To some it may appear that the wireless revolution has already made its full impact on the test and measurement industry.

After all, RF measurements topped the list of technologies test engineers were required to learn about in the past two years, according to the Test & Measurement World 2009 salary survey. Until now, many companies have been able to incrementally evolve their test architectures to absorb new RF measurement requirements. However, two critical technology trends will change this approach. First, the emergence of multiple-input multiple-output (MIMO) wireless technology, which offers significant increases in data throughput and link range without additional bandwidth or transmit power, will change test processes. Emerging communication standards based on MIMO technology include IEEE 802.11n, Mobile WiMAX Wave 2 and 3GPP Long Term Evolution (LTE). Second, the convergence of multiple wireless radios, such as GPS and WLAN, into a single system on a chip (SOC) will create new measurement requirements. While the addition of each new wireless standard delivers benefits to consumers, it creates challenges for today's test engineers. Added complexity results in longer test times and cost overruns, forcing test engineers to evaluate alternative approaches. This trend has created a new demand in the marketplace for multichannel RF testing configuration. A multichannel RF test architecture enables parallel test – that is, testing multiple wireless-enabled devices in parallel and/or testing multiple communication standards, such was Bluetooth and 3G, on the same device in parallel.

MIMO uses multiple antennas at both the transmitter and receiver. For example, a 2x2 system contains two transmitters and two receivers. A multichannel RF instrument architecture is required when fully characterizing a MIMO device during validation/verification or when implementing MIMO technology for nonproduction applications such as RADAR and beamforming. Today's 2x2 MIMO system will be an 8x8 MIMO system tomorrow, making scalability a key requirement for next-generation RF test systems. With advances in multiradio SOCs, design engineers can pack additional wireless technologies, such MIMO, into already multifaceted devices such as the next-generation smartphones. Testing a MIMO radio in production does not typically require a multichannel architecture because full spectral characterization is not required. It will, however, be one more radio that requires testing.

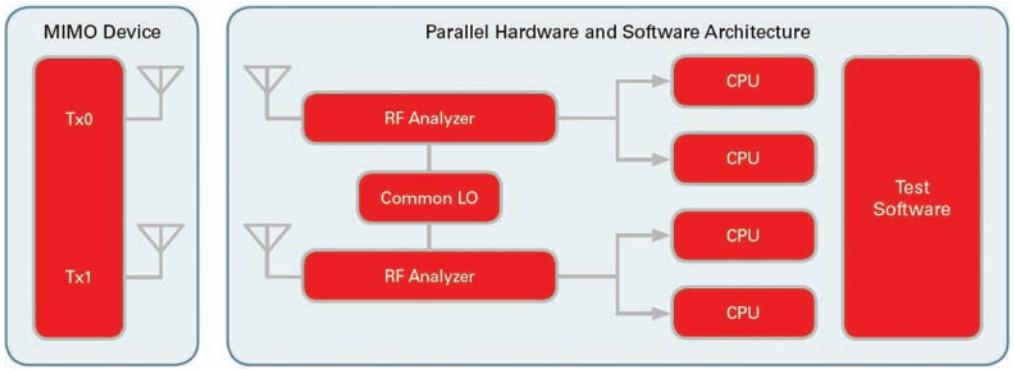

Figure 3. Multichannel RF Test System with a Parallel Phase-Coherent Architecture from Signal to Software.

To implement a parallel test architecture for multiradio devices, engineers will need RF instrumentation that can economically scale as they require more channels but is flexible enough to test multiple frequencies. This market requirement creates a need for a new class of application specific RF instrumentation with a parallel hardware and software architecture that includes advanced synchronization capabilities (see figure 3).

For example, the typical general-purpose vector signal analyzer hardware architecture is based on a three-stage superheterodyne downconversion process architecture that yields many benefits such as intermediate frequency (IF) image rejection that enables wideband acquisition on a single channel. For multichannel applications, the new class of RF instrumentation is based on simplified architectures such as signal stage downconversion and direct digital downconversion to baseband. These modern architectures and the commercial availability of low-cost, high-performance semiconductor components – such as analog-to-digital converters (ADCs)/digital-to-analog converters (DACs), field-programmable gate arrays, amplifiers, and attenuators – will reduce the cost for these instruments while preserving measurement fidelity.

In addition, the new RF instruments must be "MIMO ready," offering a new level of synchronization that goes beyond sharing signals such as the reference clock (usually 10 MHz) and the occasional start trigger. This traditional approach of synchronizing multiple RF instruments is sufficient to guarantee simultaneous signal acquisition, but it does not guarantee true phase coherency. As a result, a multichannel RF acquisition system with only a shared 10 MHz reference is characterized by substantial channel-to-channel phase skew. Achieving true phase coherency between multiple channels of RF signal acquisition requires the synchronization of all synthesized local oscillators (LOs), ADC sample clocks, and start triggers directly between each RF instrument. Instruments with this capability can achieve better than 0.1 degree channel-to-channel skew at a 1 GHz carrier frequency.

The software component of the architecture is even more important because processing a multistandard configuration is computationally intensive. The modern software architecture enables parallel data streams where one or more processing units are dedicated to each RF channel. Common parallel processing architectures found in the marketplace today include multiprocessor, hyperthreading, multicore, and FPGA. There are still additional technologies on the horizon, such as the Intel Turbo Boost technology, which is featured in the latest-generation Intel microarchitecture codenamed Nehalem. It automatically allows processor cores to run faster than the base operating frequency if it is operating below power, current, and temperature specification limits. To fully use these processor technologies, engineers need to apply parallel programming techniques such as task parallelism, data parallelism, and pipelining at both the algorithm and application software levels.

The multichannel test architecture reduces aggregate test times, increases test throughput, and improves instrument usage. But the flexibility of the architecture is just as important. For example, a MIMO configuration is typically dynamic in nature, whereas the manipulation of the phase and amplitude of each transmitter can optimize sign al performance and direction. With each additional MIMO transmitter, the software complexity increases exponentially.

In the same way that emerging wireless technologies such as MIMO antenna systems have profoundly influenced transceiver designs, they have left their mark on RF instrumentation. The multichannel wireless systems of the future will be based on a low-cost architecture that is parallel from signal to software.

Peer-to-Peer Computing

For years the computing industry has implemented distributed architectures by dividing computing among multiple processing nodes.

For example, Google search queries are not run on one single supercomputer but on a network of more than 450,000 interconnected servers. Personal computing devices run multicore processors and use specialized graphics processing units (GPUs) to handle high-definition graphics processing. With increasingly complex testing requirements and exponential growth in acquired data, automated test systems will need to evolve to work smarter and not just harder.

Peer-to-peer is a type of computing that uses a decentralized architecture to distribute processing and resources among multiple processing nodes. This is in contrast to traditional systems, which feature a central hub responsible for transferring data and managing processing. In automated test systems, peer-to-peer computing may take the form of acquiring data directly from an instrument like a digitizer and streaming it to an available field-programmable gate array (FPGA) for inline signal processing. Other systems use it to offload processing to other test systems or high-performance computers.

The trend of software-defined instrumentation is giving engineers unprecedented control over their automated test systems and opening all new types of applications. Much of this is due to the engineers' ability to access the raw measurement data, which they can analyze and process for their exact needs. With higher digitization rates and channel counts, the amount of available data is increasing at exponential rates. Within five years, some high-performance test systems will be processing petabytes (thousands of terabytes) of data per day.

Beyond the amount of data being acquired, much of it will need to be processed in real time. Applications such as RF signal processing benefit immensely if demodulation, filtering, and fast Fourier transforms (FFTs) can be implemented instantly. For example, engineers can move beyond power-level triggering in RF applications and create custom triggers based on the frequency domain of the signal.

New high-performance, distributed architectures are required to transfer and process all of this data. These new high-performance architectures will share three key characteristics:

Next-generation synthetic instruments will require high-performance signal processing while maintaining user configurability. Using peer-to-peer streaming over PXI Express, we can send acquired RF signals directly to PXI Express FPGA processing modules to realize 10X speed improvements over previous solutions.
Wade Lowdermilk, Senior Technology Fellow, BAE Systems

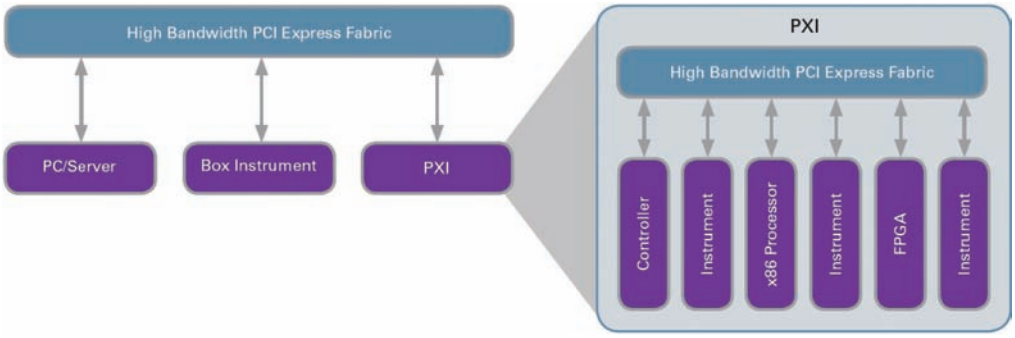

Figure 4. PCI Express is the ideal peer-to-peer architecture, enabling high-throughput and low-latency communication for automated test.

1. High-throughput, point-to-point topologies –The architecture must be able to handle the transfer of many gigabytes of data per second while allowing nodes to communicate with each other without passing data through a centralized hub.

2. Low latency – Data will need to be acquired and often acted upon in fractions of a second. There cannot be a large delay between when the data is acquired and when it reaches a processing node.

3. User-customizable processing nodes –The processing nodes must be user-programmable so that analysis and processing can meet the user's exact test system needs.

Very few distributed architectures have been able to meet all three of these criteria. For example, Ethernet provides an effective point-to-point topology with a diverse set of processing nodes, but, with high latency and average throughput, it is not well-suited to inline signal processing and analysis. The architecture that has seen the most initial success and future promise in meeting these criteria is PCI Express (see figure 4). The bus that has formed the core architecture of every PC and laptop for much of the last decade, PCI Express was specifically designed for high-throughput, low-latency transfers. It provides throughput of up to 16 GB/s (soon to be 32 GB/s) with latencies of less than a microsecond.

One place where PCI Express is already seeing use as a distributed architecture is in military and aerospace applications. In defining its next-generation test systems, the U.S. Department of Defense Synthetic Instrument Working Group identified PCI Express as the only bus capable of providing the data throughput and latency required for user-customizable instrumentation. This architecture is now seen in BAE Systems' synthetic instruments that use PCI Express to stream downconverted and digitized RF data directly to separate FPGA processing modules for inline signal processing.

Enhancements are still being made to PCI Express to further its capabilities in peer-to-peer applications. This includes bringing PCI Express out of the computer with new cabled solutions enabling low-latency communication up to 100 meters. The industry is also working to ensure that these high-performance distributed systems are compatible with components from multiple vendors. In September 2009, the PXI Systems Alliance released the PXI MultiComputing Specification to define the hardware and software interfaces to realize this goal.

Beyond just the physical architecture of these systems, peer-to-peer computing will change how engineers configure and program their test systems. With many disparate processing nodes, engineers will need new tools to visualize and direct the flow of data. Software development environments will also need to evolve to abstract away the intricacies of programming FPGAs, GPUs, x86 processors, and more.

Peer-to-peer computing using high-performance, distributed architectures is still early in its application, and there are many innovations still to come. With exponentially growing amounts of data and increasingly complex testing requirements, test engineers will need to learn how best to apply these new technologies to create smarter test systems.

To keep quality and budgets under control amidst growing product and market complexities, engineering teams should view the software and hardware test components as a common DNA that persists throughout the entire development process, from requirements definition to production test.

Phil Hester, Senior Vice President, R&D, National Instruments

Embedded Design and Test

Embedded systems and devices are providing new levels of convenience and safety to consumers.

Electronic manufacturers are equally excited by the ability to build more software-defined devices and chips that can easily be enhanced or repaired by simply installing the latest software version instead of conducting costly hardware repairs. Manufacturers are also taking advantage of the condensed hardware footprint, reduced number of physical components required by the design, and higher average selling price in many cases as a result of the increased value of the intelligent embedded devices to the customer.

As embedded devices become more ubiquitous and complex, however, embedded design and test engineers are facing significant challenges to streamline the design and test processes of embedded systems and devices. The embedded design and test process typically consists of various forms of design simulation, validation, verification, and system test. Today these phases often require a hard transition between design and test tools, which results in a complete rewrite of test code, test cases, and the simulation and I/O interfacing of the models. In addition, using traditional design tools to stitch together multiple models for simulation is becoming increasingly cumbersome with the growing complexity of the models and use cases to be examined.

Each of these issues presents real business challenges to organizations with respect to margins, time to market, required personnel, and documentation.

Hence, a growing trend in the realm of embedded design and test is the reuse of design and test tools, models, and simulation data beyond their previous silos in the development process. While many design and test engineers are actively reusing models throughout the development process, engineers can still achieve significant efficiency gains by reusing tests across the design flow as well.

Fortunately, real-time test software now offers the ability to reuse testing tasks, including stimulus profiles, test sequences, analysis routines, and requirements tracing, across the entire embedded design flow (see figure 5). This prevents the hard transition discussed above as well as the rewrite of test code between phases of the development process, which is a painful and prominent test. This provides a high degree of flexibility and adaptability when responding to any issues discovered during testing and when faced with adding further test cases resulting from project requirement changes. Lastly, some modern real-time test software tools enable the use of multicore processors to exercise many complex models and tests in parallel to produce dramatic reductions in load and test times.

As illustrated, when developing embedded control software, the stimulus profiles, analysis routines, and other components used in the model-in-the-loop (MIL) design tasks are reused to create the hardware-in-the-loop (HIL) and field tests for prototype controllers. Once this stage is complete, the evolved software test components serve as the starting point for the development of HIL, subsystem, and systems integration test systems. Ultimately, the production test plans used by manufacturing feature the same "DNA" as the original components created during the design phase.

Similarly, test benches and analyzers used by computer-aided engineering (CAE) tools in the design of ASICs are applied to instrumentation-based test systems. In the end, development teams produce and examine results the same way, allowing them to make decisions and adjustments more quickly and with greater effectiveness, which reduces the risk of schedule and budget changes.

It is important to note that while real-time test software is enabling a new level of embedded design and test efficiency, it is not the only consideration organizations should make to address their embedded design and test business needs.

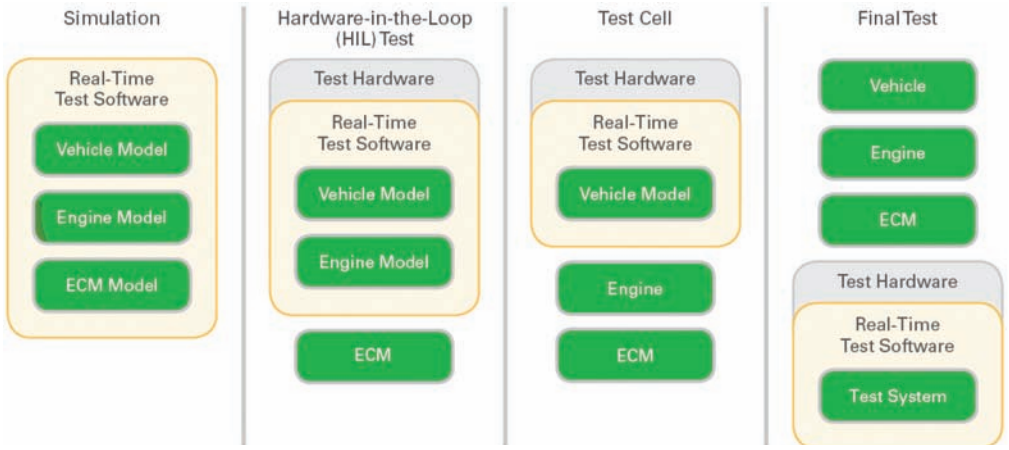

Figure 5. Real-time test software enables the reuse of models and testing tasks across the entire embedded design flow.

They should also be investing in hiring domain expertise and developing and following style guides and sophisticated processes to ensure the accuracy suitable for their development needs and the ability to synthesize real-world implementations of their designs.

In essence, the companies that are most likely to remain competitive are those that view their test tasks as offshoots of the procedures used during the creation of the product. While they inherently have different goals, the subsequent test components will share a common ancestry – in some cases being a clone of the previous steps and in others an evolution. This relationship expands beyond the common origin of project requirements that it is today to the actual reuse of test components and processes, resulting in significant cost, time, and personnel savings while delivering the improved quality of life users have come to expect from the latest embedded devices.

Reconfigurable Instrumentation

Test systems are reconfigured for endless reasons – from adapting to new test requirements to accommodating instrument substitutions during calibration and repair cycles.

Software-defined instrumentation, also known as virtual instrumentation, is based on a modular architecture that enables a high degree of reconfigurability. Software-defined instruments consist of modular acquisition/generation hardware whose functionality is characterized through user-defined software running on a host multicore processor.

This basic model is ideal for most automated test applications in use today, but new technologies and test methodologies on the horizon are creating the need to push the reconfigurability down to the hardware to achieve required performance. One example of this is testing a modern RF receiver, where coding/ decoding, modulation/ demodulation, packing/unpacking, and other data-intensive tasks may need to occur inside a clock cycle of the device under test (DUT). In these cases, the software defined architecture needs to be flexible enough to incorporate user-programmable hardware – often a field-programmable gate array (FPGA) – to place the necessary intelligence inside the instrument. User-programmable instruments create an architecture where data can be acted upon in real time on the FPGA and/or processed centrally by the host processor (see figure 6).

FPGAs are a key enabling technology because they combine the best parts of ASICs and processor-based systems. At the highest level, FPGAs are reprogrammable silicon chips. Using prebuilt logic blocks and programmable routing resources, engineers can configure these chips to implement custom hardware functionality. They can develop digital computing tasks in software and compile them down to a configuration file or bit stream that programs the FPGA components.

The ability to customize the measurement hardware itself represents yet another milestone in the path toward a completely software-defined test system. In 10 years, we will wonder how we ever programmed test systems effectively without this capability.
Mike Santori, Business and Technology Fellow, National Instruments

In addition, FPGAs are completely reconfigurable and instantly take on a new personality when recompiled with a different configuration of circuitry.

Beyond being user-programmable, FPGAs offer hardware-timed execution speed as well as high determinism and reliability. They are truly parallel so different processing operations do not have to compete for the same resources. Each independent processing task has its own dedicated section of the chip, and each task can function autonomously without any influence from other logic blocks. As a result, adding more processing does not affect the performance of another part of the application.

While FPGAs have been used inside instruments for over a decade, test engineers were seldom given access to embed their own algorithms on them. To be useful in a software-defined instrumentation context, FPGAs must be reprogrammable by the engineer in software; in other words, they should be used to push software programmability down into the hardware itself. In the past, FPGA technology was available only to engineers with a deep understanding of digital hardware design software, such as hardware description languages like Verilog or VHDL, which use low-level syntax to describe hardware behavior. Most test engineers do not have expertise in these tools. However, the rise of high-level design tools is changing the rules of FPGA programming, with new technologies that convert graphical block diagrams or even C code into digital hardware circuitry. These system-level tools that abstract the details of FPGA programming can bridge this gap.

Clearly, there are advantages to performing different types of processing on a host processor versus an FPGA. For example, an FPGA is generally well-suited for inline analysis such as simple decimations on point-to-point I/O, whereas complex modulation might achieve better performance running on a multicore processor due to the large amount of floating-point calculations required. The ideal solution for developing a software-defined test system is a single graphical system design development environment that provides the ability to quickly partition the processing on the host or an FPGA to see which offers superior performance.

This new software-defined architecture can meet application challenges that are impossible to solve with traditional methods such as the previous example that requires real-time decision making by the host to properly test the device. Instead, engineers can fully deploy the intelligence to the FPGA embedded on the instrument for pass/fail guidance. This is often the only way to supply the intense timing and determinism required by the DUT. Examples of this type of device include RFID tags, memory, microcontrollers, and engine control units (ECUs). For some applications, engineers also perform the communication over a protocol – wireless or wired – which requires a significant layer of coding and decoding before making a decision.

Reconfigurable instruments will continue to find more mainstream applications as test engineers continue to look for creative ways to reduce test time and system cost. Take, for example, a digitizer that has an FPGA inline with an analog-to-digital converter. An engineer can deploy functions to the FPGA such as filtering, peak detection, fast Fourier transforms (FFTs), or custom triggering. Not all data is created equal, but an FPGA-based digitizer can make quick decisions on which data is worthless and can be discarded and which data has value. This can ultimately reduce measurement time substantially. Test engineers in the military and aerospace industry have been early adopters of FPGA-based instrumentation through their synthetic instrumentation initiatives, but this technology also has potential for telecommunications, automotive, medical device, and consumer electronics applications.

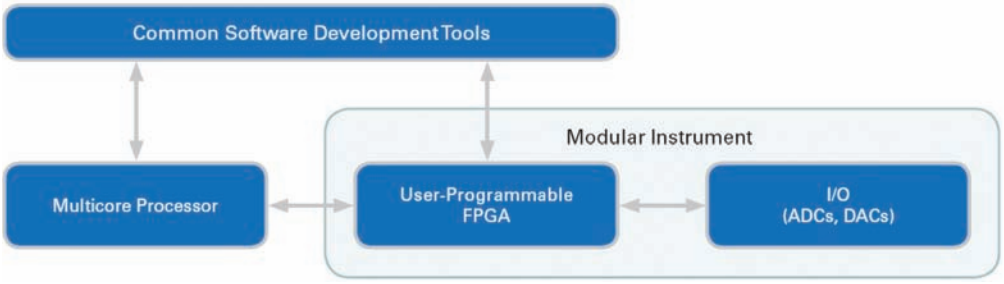

Figure 6. Reconfigurable instruments provide a Host + FPGA configuration that delivers both performance and flexibility.